Logical & Bit operations (In Assembly Language) Exercises

1. Set port 0, bits 1,3, 5 and7, to 1; set the rest to 0.

CSEG AT 0

SETB C

MOV A,P0

CLR A

MOV ACC.1,C

MOV ACC.3,C

MOV ACC.5,C

MOV ACC.7,C

MOV P0,A

END

(OR)

CSEG AT 0

MOV A,#0AAH

MOV P0,A

END

1. Clear bit 3 of RAM location 22h without affecting any other bit.

CSEG AT 0

MOV 22H,#35H

CLR 22H.3

END

(OR)

CSEG AT 0

MOV 22H,#35H

MOV A,22H

CLR ACC.3

MOV 22H,A

END

1. Invert the data of the port 0 pins and write the data to port 1.

CSEG AT 0

MOV P0,#45H

MOV A,P0

CPL A

MOV P1,A

END

1. Swap the nibbles of R0 and R1 so that the low nibble of R0 swaps with the high nibble of R1 and the high nibble of R0 swaps with the low nibble of R1.

CSEG AT 0

MOV R0,#45H

MOV A,R0

SWAP A

MOV R2,A

MOV R1,#35H

MOV A,R1

SWAP A

MOV R0,A

MOV A,R2

MOV R1,A

END

1. Complement the lower nibble of RAM location 2Ah.

CSEG AT 0

MOV 2AH,#45H

CPL 2AH.0

CPL 2AH.1

CPL 2AH.2

CPL 2AH.3

END

(OR)

CSEG AT 0

MOV 2AH,#45H

XRL 2AH,0FH

END

1. Make the high nibble of R5 the complement of the low nibble of R6.

CSEG AT 0

MOV R5,#35H

MOV R6,#45H

MOV A,R6

CPL ACC.0

CPL ACC.1

CPL ACC.2

CPL ACC.3

MOV 20H,A

MOV A,R5

SETB C

ANL C,20H.0

MOV ACC.4,C

CLR C

CPL C

ANL C,20H.1

MOV ACC.5,C

CLR C

CPL C

ANL C,20H.2

MOV ACC.6,C

CLR C

CPL C

ANL C,20H.3

MOV ACC.7,C

MOV R5,A

END

1. Move bit 4 of RAM location 30h to bit 2 of A.

CSEG AT 0

MOV 30H,#45H

MOV C,30H.4

MOV ACC.2,C

END

1. Store the least significant nibble of A in both nibbles of RAM address 3Ch; for example, if A=36h, then 3Ch == 66h.

CSEG AT 0

MOV A,#36H

ANL A,#0FH

MOV 20H,A

MOV A,#36H

ANL A,#0FH

SWAP A

ORL A,20H

MOV 3CH,A

END

1. Set the Carry flag to 1 if the number in A is even; set the Carry flag to 0 if the number in A is odd.

CSEG AT 0

CLR C

MOV A,#46H

RRC A

MOV 20H,C

END

1. Treat registers R0 and R1 as 16-bit registers, and rotate them on place to the left; bit 7 of R0 becomes bit 0 of R1, bit 7 of R1 becomes bit 0 of R0, and so on.

CSEG AT 0

MOV R0,#85H

MOV R1,#87H

MOV A,R0

RLC A

MOV R0,A

MOV A,R1

RLC A

MOV R1,A

MOV 20H,R0

MOV 20H.0,C

MOV R0,20H

END

1. Reverse the bits of R0 registers.

CSEG AT 0

MOV R0,#85H

MOV 20H,R0

MOV C,20H.0

MOV 21H.0,C

MOV C,20H.7

MOV 20H.0,C

MOV C,21H.0

MOV 20H.7,C

MOV C,20H.1

MOV 21H.1,C

MOV C,20H.6

MOV 20H.1,C

MOV C,21H.1

MOV 20H.6,C

MOV C,20H.2

MOV 21H.2,C

MOV C,20H.5

MOV 20H.2,C

MOV C,21H.2

MOV 20H.5,C

MOV C,20H.3

MOV 21H.3,C

MOV C,20H.4

MOV 20H.3,C

MOV C,21H.3

MOV 20H.4,C

MOV R0,20H

END

1. Rotate the DPTR one place to the right

CSEG AT 0

MOV DPL,#45H

MOV DPH,#25H

CLR C

MOV A,DPH

RRC A

MOV A,DPL

RRC A

MOV DPL,A

MOV A,DPH

RRC A

MOV DPH,A

END